Two Efficient Ternary Adder Designs Based On CNFET Technology*

Research Article

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Abstract: Full adder is one of the essential circuits among the various processing elements used in VLSI and other technologies circuits, because they are mainly employed in other arithmetic circuits, such as multi-digit adders, subtractors, and multipliers. This paper proposes two efficient ternary full adders based on Carbon Nanotube Field-Effect Transistor (CNFET) technology. Using the adjustable nanotube diameter in CNFETs, these adders utilize arbitrary threshold voltages so that arithmetic operations can be performed with a radix of 3. For performance analysis, the proposed adder circuits are simulated in HSPICE with 32nm CNFET technology. In these simulations, different inputs are applied at different frequencies with different load capacitances placed at the output. Simulation results have shown that the proposed adders not only improve the speed, power consumption, and Power Delay Product (PDP) of the existing state-of-the-art designs but also improve the design complexity by reducing the number of transistors contained within the circuit.

Keywords: CNFET, Ternary Adder, Multi-Value Logic, Ternary Logic, Nanotechnology.

1. Introduction

In recent decades, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology has played a significant role in the development of high-density Very-Large-Scale Integration (VLSI) circuits [1] . This technology offers low energy consumption and high performance at reasonable scales. One of the main strategies for improving efficiency in digital circuits is transistor miniaturization, but in the case of MOSFETs, this strategy now faces some challenges, such as high power densities, reduced gate control, short channel effects, and high sensitivity to process variations [2, 3]. Frustrated by these limitations, researchers have shown increasing interest in possible alternative technologies, such as single electron transistors [4], Quantum Cellular Automata (QCA) [5,6], fin field-effect transistor (FinFET) [7&8] and Carbon Nanotube Field Effect Transistors (CNFET) [3&9]. Among these technologies, CNFET offers unique features that make it one of the best alternative to MOSFET [10-12].

Since the structure of the conventional MOSFET and CNFET are very similar, the design and implication of CNFET circuits can be done without making any significant changes in CMOS-based circuits [9].

The notable unique features of CNFETs include one-dimensional band structure which suppresses backscattering, near ballistic operation, and similar mobility of PFET and NFET transistors which make transistor sizing easier [10].

These properties have made it possible for many researchers to use CNFET to design and implicate VLSI circuits, such as adders [3, 11, 13], multipliers [14], compressors [12], flip-flops [15, 16] and SRAMs [2, 8, 17, 18].

One of the exceptional features of CNFETs is that their threshold voltage can be easily controlled by changing the diameter of nanotubes [11&13]. This unique feature makes CNFETs the best candidate for designing Multi-Value Logic (MVL) circuits [11,13] because the standard design of MVL circuits involves using multiple voltage thresholds, which in CNFET can be easily achieved by adjusting the nanotube diameter [11&13]. Unlike binary logic, MVL works with more than two levels of logic, thus allowing logical and arithmetic operations to be performed on more than two logical values [3, 10]. Hence, with MVL, many logical operations can be performed in fewer steps and at higher speeds. The binary logic also imposes performance limitations as it requires a significant area of VLSI chip to be dedicated to connections (about 70% to connections, about 20% to insulation, and about 10% to the device itself) [19]. To circumvent this limitation, some researchers have attempted to design MVL circuits with CNFET technology [10, 13, 20].

Among the basic blocks of arithmetic circuits, digital adders are particularly important because of their use in other computational circuits such as multi-digit adders, subtractors, and multipliers [10&20]. Therefore, an improvement in the performance of adder circuits will enhance the performance of other circuits as well. More detailed information about the existing designs for adder circuits can be found in [3, 9, 10, 21].

This paper presents two new Ternary CNFET-based adders, which offer not only lower power consumption but also better PDP than the existing designs. The basis of the proposed full adder circuits is the control of the final transistors by the branches of the transistors, so that, according to the summation of inputs, the correct value is generated in the output of the circuits.

In the rest of this paper, Section 2 gives a brief introduction to CNFET technology, Section 3 explains the ternary logic and how an extra-logical value is introduced in

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CNFET, Section 4 reviews the previous works done in this area, Section 5 describes the proposed full adders, and Section 6 presents the simulation results and makes a comparison with other adders. Finally, Section 7 concludes the paper.

2. Carbon Nanotube Field Effect Transistors

Carbon Nano-Tube (CNT) was discovered in 1991 by S. Iijima. CNT is a Nano-scale tube which is made of a rolled sheet of graphene. In other words, a CNT can be viewed as a graphene sheet that has been rolled into a tube. This transformation can be expressed with the vector where are the unit vectors of the graphene lattice and are positive integers that determine how the carbon sheet is rolled [3, 9].

The diameter of the carbon nanotube is given by:

$$D_{cnt} = \frac{\alpha \times \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \qquad (1)$$

where α is the distance between carbon atoms [3].

Since CNTs are graphene sheets rolled around a vector [19], the nanotube diameter can be adjusted by changing the size and direction of this vector and the placement of atoms around the nanotube axis.

So far, three types of CNT transistor have been proposed [3]. The first type is the Schottky barrier (SB) CNFET, which consists of metal-semiconductor and CNT-metal contacts and operates by direct tunneling from the Schottky barrier formed at the source/drain-channel contact (metal and CNT). The main problem of this type of CNT transistor is that the formation of Schottky barrier in the CNT-metal contact limits the transconductance in the ON-state and undermines the current conductivity, which is a critical factor for high-speed operations and also reduces the drain current. Moreover, some features of this type of transistor limit its use in conventional logic families. This type of transistor is ill-suited for medium and high-performance applications. The second type of CNT transistor is Tunneling Carbon Nanotube Field-Effect Transistor (T-CNFET). This type of transistor maintains low current in the ON-state, which makes it suitable for low-power and sub-saturation applications but not for high-speed ones. The third type of CNT transistors is known as MOSFET-like CNFET. These CNFETs offer a compromise between high-speed and low power consumption. The main advantage of these transistors is the absence of a Schottky barrier in the source-channel contact, which results in substantially high current in the ON-state, causing them to behave like a MOSFET and exhibit unipolar behavior. Another advantage of MOSFET-LIKE CNFETs is their high scalability compared to the alternatives, which makes them very suitable for digital applications that require high-performance transistors [3]. Figure 1 illustrates the structure of different types of CNFET.

Given the reviewed advantages and disadvantages of different types of CNFET, it can be concluded that the similarity of MOSFET-LIKE CNFETs to MOSFETs in terms of performance and intrinsic properties make them the best choice for the proposed circuits. In this paper, MOSFET-LIKE CNFETs used for designing efficient adders.
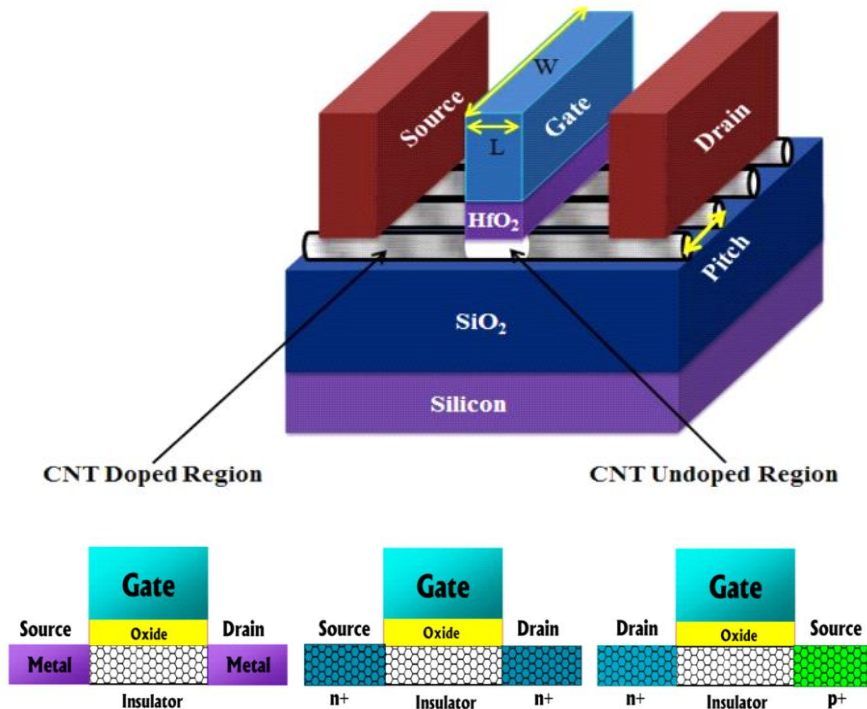

Figure 1. Three different types of CNFET [22]

3. Ternary Logic

MVL systems offer many advantages over binary systems. Most notably, this logic allows us to achieve higher data processing capacity per unit, reduces the number and complexity of connections among modules and the number of active devices within a chip. Thanks to these advantages, the circuits designed with MVL are more straightforward, more flexible, and more compact [3]. In practice, using MVL increases the speed and reduces the area and power consumption of the chip. For example, if used correctly in the design of a multi-valued multiplier, MVL can make up to 50% reduction in chip area and power consumption compared to binary alternatives [23]. Another advantage of MVL is the reduction in memory size because the bigger radix needs fewer memory cells to store the data [23].

In a conventional binary system, we have two logical values '0' and '1', which are represented by 0V and Vdd, respectively. In a ternary logic system, valid values are '0', '1' and '2', which are represented by 0V, Vdd/2, and Vdd, respectively.

In general, the smaller radix needed to the larger number of digits to express a quantity. The number of digits needed to express a range is given by $N = R^d$, where R is the radix and d is the number of needed digits, which must be rounded to the largest integer needed. Assuming that the hardware cost and complexity of the system, C is proportional to the digital capacity R*d, it follows that:

$$C = k(R \times d) = k \left[R \frac{logN}{logR} \right] \tag{2}$$

where k is a constant value. By differentiating this equation concerning R, it can be deduced that to obtain the lowest cost (C), R should be equal to e = 2.718. Since R must be an integer, it is recommended to use R = 3 (ternary), which is more efficient than R = 2 [24].

A ternary adder is a logic circuit that receives three input values *a*, *b*, *c* and produces two outputs *sum* and *carry* based on ternary logic. Naturally, *sum* represents the sum of values and *carry* represents the carry trit (ternary bit). The truth table of a ternary adder is provided in Table 1 [19].

Table 1. Truth table of a ternary adder [9]

A+B+Cin	sum	Cin
0	0	0
1	1	0
2	2	0
3	0	1
4	1	1
5	2	1
6	0	2

As mentioned, many CNFET-based arithmetic circuits have been designed so far. Given that full adder is a primary arithmetic circuit frequently used in the design of other circuits, researchers have also proposed a variety of ternary full adder circuits based on CNFET technology. These circuits can be divided into three groups: the first group is the circuits that use ternary logic in data exchange but perform the operations with binary logic gates. This method of using ternary logic only reduces the number of connections and related contacts, and also imposes a longer critical path, which results in long delays compared to other designs. An excellent example of such circuits is the one proposed in [25]. The second group consists of circuits that make use of two power supplies in their design and allow each logic level to draw from one power supply. These circuits have low power consumption, but the presence of two power supplies complicates the layout design, as each power supply should be connected to all modules (digital circuits), and even then it would be very difficult to connect the modules. The design presented in [10] is an excellent example of these circuits. The last group is the circuits that perform arithmetic operations with ternary logic but have only one power supply. In these circuits, the required logical levels are generated using the unique features of CNFETs. Examples of this approach are the designs proposed in [10] and [20]. The third approach was chosen for the development of the proposed ternary adder circuits, due to its advantages.

As mentioned earlier, ternary circuits have one more logic value than binary circuits. In CNFET-based circuits, the voltage of this value can either be provided by an extra power supply or be generated by the circuit itself. Since adding an extra power supply complicates the layout design, it is preferable to generate all valid values within the circuit itself. Since Vdd is equivalent to logical 2 and GND represents logical 0, it is enough to generate Vdd/2 as the voltage level equivalent to logical 1. There are several ways to generate logical value 1 with CNFET technology. In order to minimize the impact on circuit speed and size, it is customary to use transistors for this purpose. in Figure 2 resents three conventional methods of generating logical 1 in CNFET-based ternary circuits. In this figure, only the general scheme of creating logical 1 is given.

The circuit illustrated in Figure 2-a operates like two weak resistors that give half of the supply voltage at the output. In this method, there is no need to have an extra path for generating logical 2 or 0 to the output, because for logical 0, the output can be connected to the earth through the NFET transistor, and for logical 2, it can be connected to the power supply through the PFET transistor [26]. This method can reduce the number of transistors for some circuits, for example, the standard ternary buffer can be implemented with only six transistors, but it has a high power consumption because of the way logical 1 is generated (as mentioned, it resembles the use of two weak resistors). The circuit shown in Figure 2-b generates the logical 1 in the same way but has a lower power consumption because transistor gates are connected to the drain, thus creating more resistance than the previous design [9]. However, this approach requires having separate paths for connecting the output to the power supply and the earth, because neither NFET nor PFET will be fully saturated to pass the voltage correctly.

Consequently, more transistors will be needed than the first method. The third method of generating logical 1 is to connect the source of NFET to the high voltage, the source of PFET to the low voltage, and the drain of both transistors

to the output. In this approach, both transistors will always be ON [26]. This method allows us to avoid having separate paths for logical 0 and 2 but requires more transistors than the first method for some circuit. Nevertheless, it has a lower power consumption than both alternatives [26]. Figure 2c shows the circuit of this method.

Table 2 shows the power consumption and the output voltage level of the above-described circuits in the generation of logical 1 according to a 100-nanosecond simulation conducted using the parameters given in Table 4 with a 1fF load capacitance (at the output) and a 0.9v power supply. In this simulation, only transistors that create logic 1 are used, and the inputs were set such that the circuit would produce logical 1 at the output. Given the lower number of transistors for some circuit in the first method Figure 2a and the lower power consumption of the third method Figure 2c, the ternary adder circuits of this paper were designed based on these two approaches.
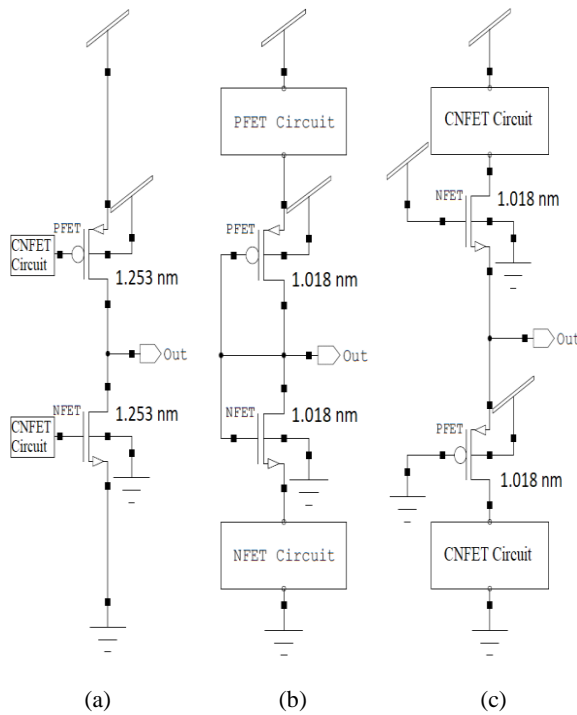

Figure 2. Circuits for generating logical 1 with CNFET technology

Table 2. Comparison of the methods for generating logical 1 with CNFET technology

Methods	Power Consumption (W)	Voltage level on output(V)
a)	2.8238e-5	0.4351
b)	1.6255e-7	0.3767
c)	1.5552e-8	0.5115

4. Previous Works

Given the importance of adder cells as basic blocks of digital systems and the explained benefits of multi-valued logic, researchers have proposed various designs for the implementation of ternary adders with CNFET technology [3,9,10,20,21]. In the following paragraphs, the prominent proposals in this area are briefly reviewed.

The first two CNFET-based ternary adders were introduced in [3]. This first circuit produces the inverse of outputs (sum and Cout) and then uses a ternary inverter to produce the correct sum and Cout. Given how the output is generated, this design has a longer critical path than the other design but also has a lower power consumption. This design has 24 CNFETs and five capacitors, but the second design contains only 18 CNFETs with the same number of capacitors, as it uses a buffer circuit to reduce the length of the critical path. As a result, the second ternary adder has a higher power consumption but lower delay.

In [9], a ternary adder based on a ternary decoder was developed. In this adder, the input values are given to a decoder, which produces the binary equivalents to be used in binary arithmetic operations. The results of these binary operations are then converted to ternary values using ternary buffers and encoders.

In [21], this design was improved by using an improved encoder and a fast carry generation to reduce delay and consequently, PDP.

In [20], a ternary adder was developed by embedding multiplexers in the design. In this design, the derivatives of input A are connected to three initial multiplexers, and input B acts as the selector for these multiplexers, and the outputs of these multiplexers are connected to the input of the last multiplexer for which the input C is the selector. The only difference between the adder circuit and the carry circuit is in the inputs of the three initial multiplexers.

[10] presented two ternary adders, both using Transmission Gates (TG) and ternary inverters. In the first design, the output of two serially connected ternary inverters is connected to the TGs to generate the sum. However, the second design uses a single ternary buffer instead of serial inverters. Both designs contain three capacitors, but while the first one has 55 CNFETs, the second one has 43 CNFETs. Hence, the second ternary adder occupies less space and also has a lower delay because of using a ternary buffer.

The present paper introduces two efficient ternary adder circuits inspired by the designs presented in [10].

5. Proposed Work

This section presents the proposed adder circuits. In ternary full adder circuits, the relationship of values and sum can be expressed as follows [10]:

$$\sum in = A + B + Cin = 3Cout + sum \qquad (3)$$

From this formula, it follows that:

$$sum = \sum in - 3Cout \qquad (4)$$

In these equations, *A* and *B* are the inputs given to the adder, C_{in} denotes the input carry, C_{out} denotes the output carry (with a weight of 3), and *sum* denotes the sum. Equation (3) is similar to the division operation formula given in Equation (5). This similarity is used to obtain new relationships for the design of the adder circuit.

$$X = QD + R \ \ with \ R < D \tag{5}$$

The multiplier 3 in Equation (3) can be considered equivalent to the quotient, C_{in} can be considered equivalent to the divisor, and *sum* can be considered equivalent to the remainder. Under these assumptions, Equation (6) can be deduced.

$$\begin{cases} sum = \sum in \ mod \ 3 \\ \ C_{out} = \left\lfloor \dfrac{\sum in}{3} \right\rfloor \end{cases} \tag{6}$$

In Equation (6), the sign ⌊ ⌋ is used to show that the result of the division should be rounded down to give an integer. Thus, the following can be deduced for C_{out}:

$$C_{out} = \begin{cases} 0 & 0 \le \sum in \le 2 \\ 1 & 3 \le \sum in \le 5 \\ 2 & 5 < \sum in \le 6 \end{cases} \tag{7}$$

Also, from Equations (3) and (7), it follows that:

$$sum = \sum in - 3C_{out} = \begin{cases} \sum in & 0 \le \sum in \le 2 \\ \sum in - 3 & 3 \le \sum in \le 5 \\ \sum in - 6 & 5 < \sum in \le 6 \end{cases} \tag{8}$$

The term $\frac{\sum in}{3}$ in these equations is implemented with the capacitors, as shown in Figure 3. In circuits, this term is called *Min* and is given as input. For the rest of digital circuits, it is implemented at the transistor level. The *carry* circuit returns logical 0 if the sum of inputs is less than 2.5, returns logical 1 if this sum is greater than 2.5 but smaller than 5.5, and returns logical 2 if this sum is greater than 5.5. The input value identification and arithmetic operations are realized by the adjustment of nanotube diameters in the carry circuit. The carry circuits of the first and second proposed full adders are illustrated in Figure 4 and 5, respectively. As shown in these figures, the two middle signals of the carry circuits, which are called j and k, are used as the inputs of ternary full adders. The first ternary full adder makes use of the carry circuits proposed in [10]. But for the second full adder, the carry circuit is specially designed to a minimum the number of transistors as well as power consumption.

Figure 6 displays the circuit of the first proposed adder. The output of this adder is produced by the transistors *T1*, *T2*, and *T3*. The input Min controls the transistor T3, and the other two transistors are controlled by a circuit. The chirality of each transistor is printed beside it. The chirality of *T3* is set such that it will switch ON only if the sum of the values is greater than 5.5. The controller circuits of *T1* and *T2* are split into several branches, each of which is activated at specific logical values to switch the transistor ON or OFF. The name assigned to each branch is printed beside it. For example, if the sum of inputs is logical 4, then the transistors of the branches US4 and DS3 will be switched ON, which means T1 and T2 will be switched ON to generate logical 1 at the output. The relationship of the branches with the sum of inputs is described in Table 3. The operation of transistors T1 and T2 are based on the first method presented in section 3.

Figure 7 shows the second ternary full adder. This adder is similar to the first one, and the only difference is that *T1* and *T2* are replaced, respectively, with the circuits *C1* and *C2* to reduce the power consumption. Circuits C1 and C2 work according to the third method presented in section 3.
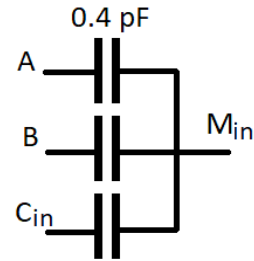

Figure 3. Arrangement of capacitors in the proposed full adders
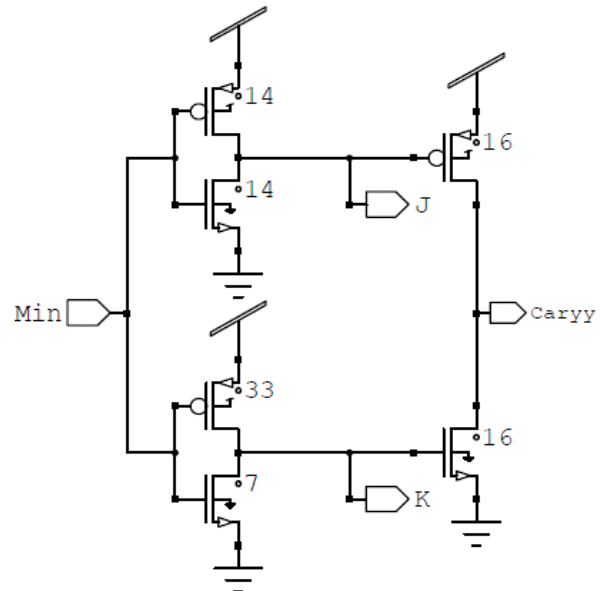

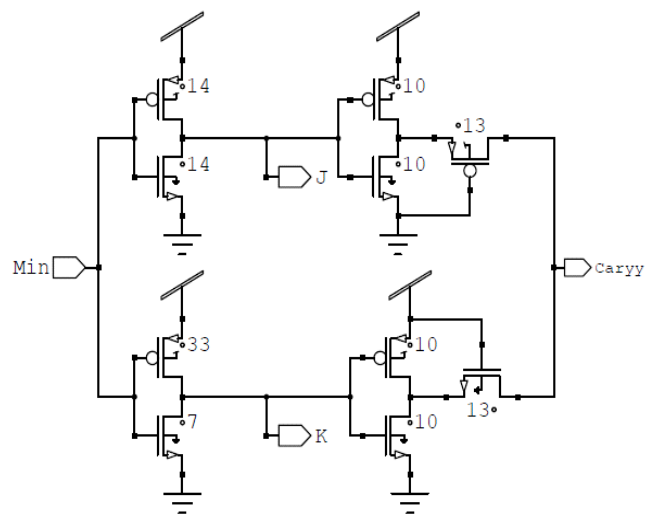Figure 4. Carry circuit of the first proposed ternary full adder

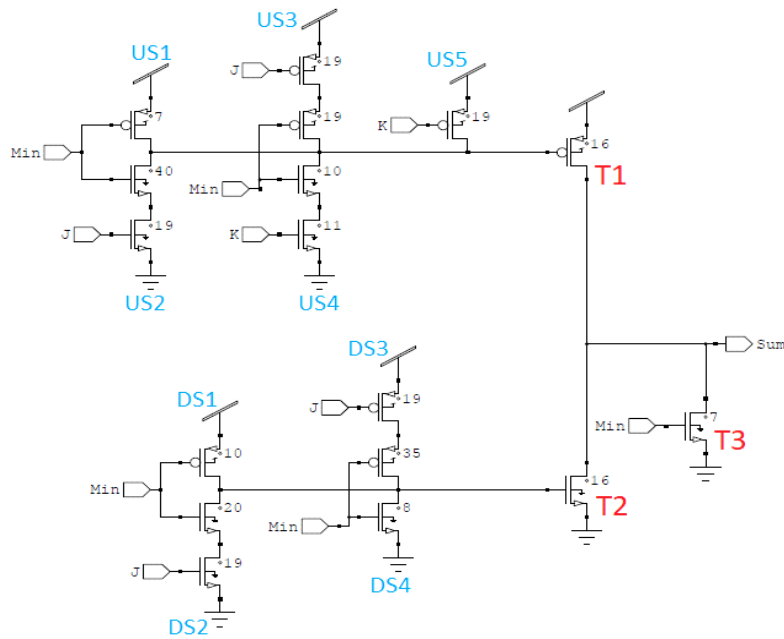Figure 5. Carry circuit of the second proposed ternary full adder

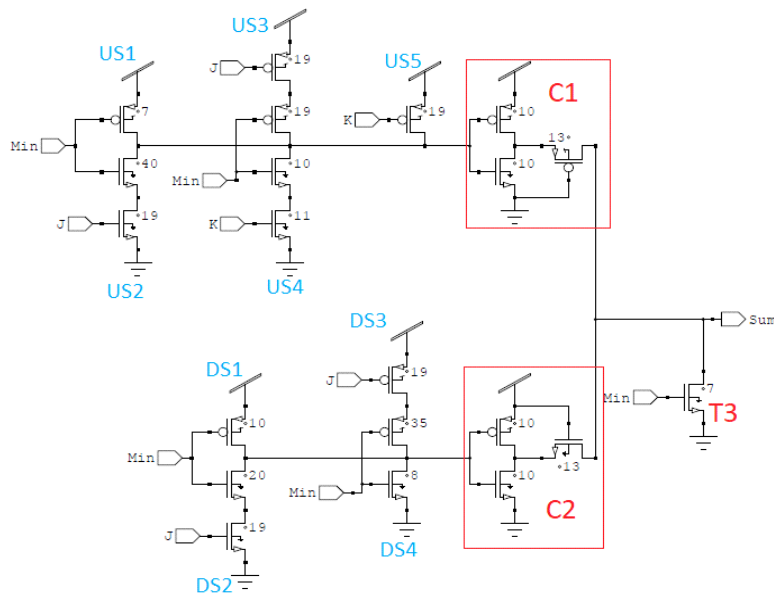Figure 6. The first proposed ternary full adder

Figure 7. The second proposed ternary full adder

Table 3. Relationship of the branches with the sum of inputs

A+B+Cin	Up Stems	Down Stems	T1 (C1)	T2 (C2)	T3
0	US1	DS1	Off	On	Off
1	US2	DS1	On	On	Off
2	US2	DS2	On	Off	Off
3	US3	DS3	Off	On	Off
4	US4	DS3	On	On	Off
5	US4	DS4	On	Off	Off
6	US5	DS4	Off	Off	On

6. Simulation Results

This section presents the details and results of the simulations of the proposed ternary adder circuits and the comparison made with the circuits proposed in [20] and [10] in terms of the number of transistors, delay, power consumption, and energy. The simulations were conducted in the software HSPICE 2014 using the Stanford University CNFET library based on 32-nm technology [27]. This library is modeled on physical experiments that verify it. The simulations of the CNFET technology were performed using the parameters listed in Table 4.

The full adders of [10] create different values based on the sum of inputs and formulas (7) and (8). Then, they indicate which path to the output must be selected in order to

accomplish the correct result. However, the full adders proposed in this paper perform the summation of the inputs by activating the different branches (paths) based on the sum of the inputs and by controlling the transistors that create the result.

The ternary adder circuits simulated with a 0.9v power supply, frequency of 250MHz, and a load capacitance of 1fF at the output. Table 5 resents simulation results.

Figure 8 displays the output transient waveforms of the proposed full adders for various inputs, which confirm they operate correctly. A comparison is also made between the performances of the proposed full adders under the load capacitances ranging from 0fF to 5fF. The diagrams of these comparisons are plotted in Figure 9, 10, and 11. The results of applying different levels of voltage with the frequency of 250 Mhz and the load capacitance of 1 fF to the full adder circuits are shown in Figure 12, 13, and 14.

As shown in Table 5, the first proposed adder is the fastest adder circuit at both 250MHz and 100MHz frequencies. More precisely, this adder is 8% faster at 250 MHz frequency and 10% faster at the 100 MHz frequency than the fastest state-of-the-art adder in the literature (the adder of [10]). Regarding power consumption, at both 250MHz and 100MHz frequencies, the second proposed full adder consumes 11% less power than the second (power saving) adder of [10]. At 250MHz and 100MHz frequencies, the second proposed full adder also achieves, respectively,

21% and 18% better PDP than the first adder of [10]. Note that these improvements have been achieved while the first and second proposed adders are respectively 47% and 28% less complicated than the second adder of [10] in terms of the number of transistors contained within circuits. As the diagram plotted in Figure 11 shows, the proposed adders are also more stable against changes in the load capacitance at the output.

Table 4. Important parameters of the CNFET model

Lch	Physical channel length	32 nm
Lgeff	The mean free path in the intrinsic CNT channel	100 nm
Lss	The length of doped CNT source-side extension region	32 nm
Ldd	The length of doped CNT drain-side extension region	32 nm
Kgate	The dielectric constant of high-k top gate dielectric material	16
Tox	The thickness of high-k top gate dielectric material	4 nm
Csub	The coupling capacitance between the channel region and the substrate	20 pF/m
EFI	The Fermi level of the doped S/D tube	6 eV

Table 5. Results of the simulation of ternary full adders

| Frequency = 250 MHz, Load = 1 fF, Vdd=0.9v					Frequency = 100 MHz, Load = 1 fF, Vdd=0.9v				
Designs	# of transistors	Delay (e-10s)	Power (e-5 W)	PDP (e-15 J)	Designs	# of transistors	Delay (e-10 s)	Power (e-5 W)	PDP (e-15 J)
Proposed 1	23	0.512	1.84	0.942	Proposed 1	23	0.505	1.94	0.98
Proposed 2	31	0.589	0.928	0.547	Proposed 2	31	0.613	0.911	0.558
Design 1 of [10]	55	0.665	1.04	0.692	Design 1 of [7]	55	0.665	1.02	0.676
Design 2 of [10]	43	0.555	1.84	1.02	Design 2 of [7]	43	0.559	1.93	1.08
Design of [20]	105	0.681	1.79	1.21	Design of [22]	105	0.731	1.85	1.35
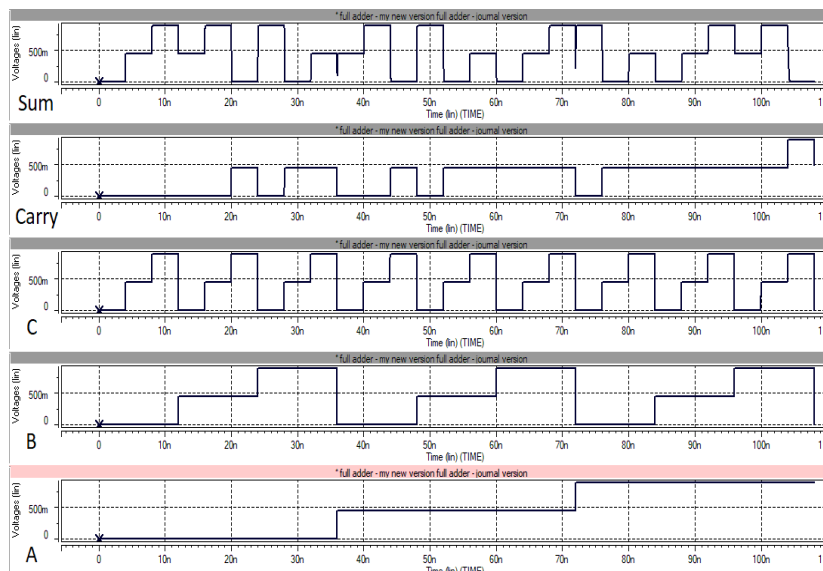
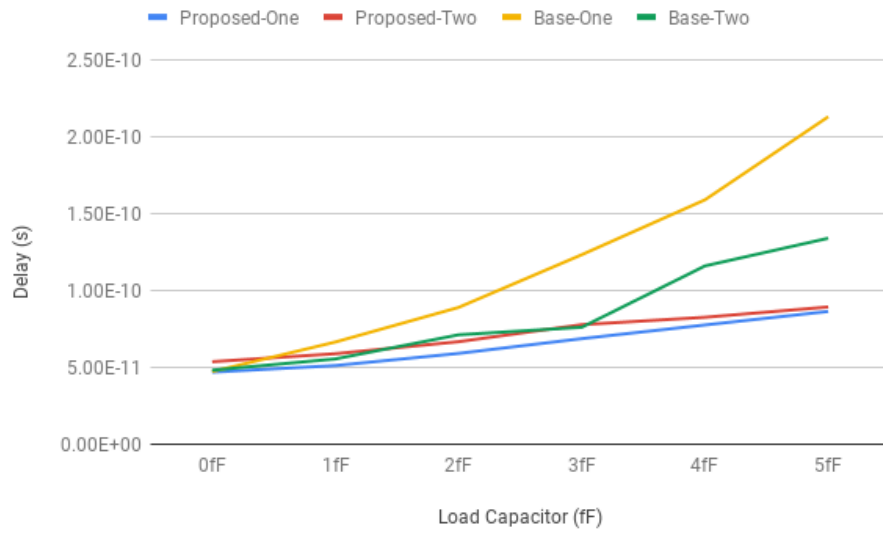Figure 8. Transient waveforms of the simulated full adders.

Figure 9. Diagram of delay versus load capacitance (at the output)
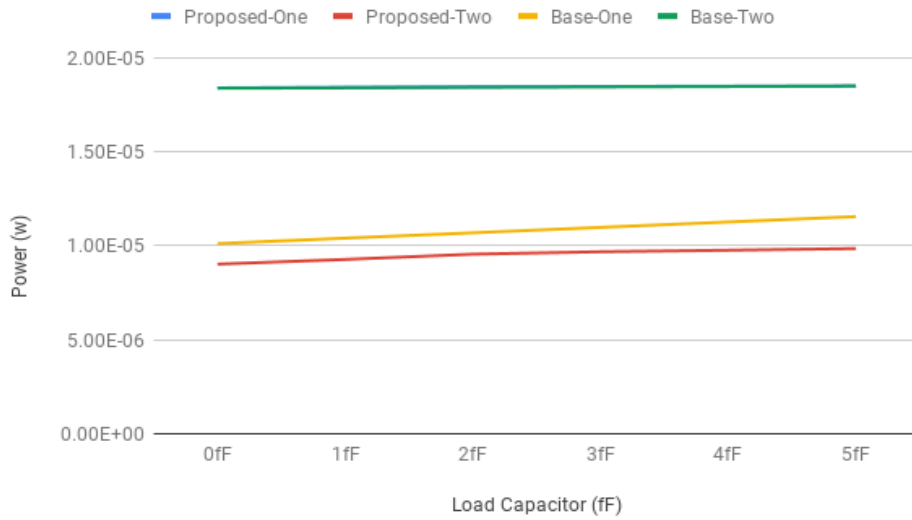
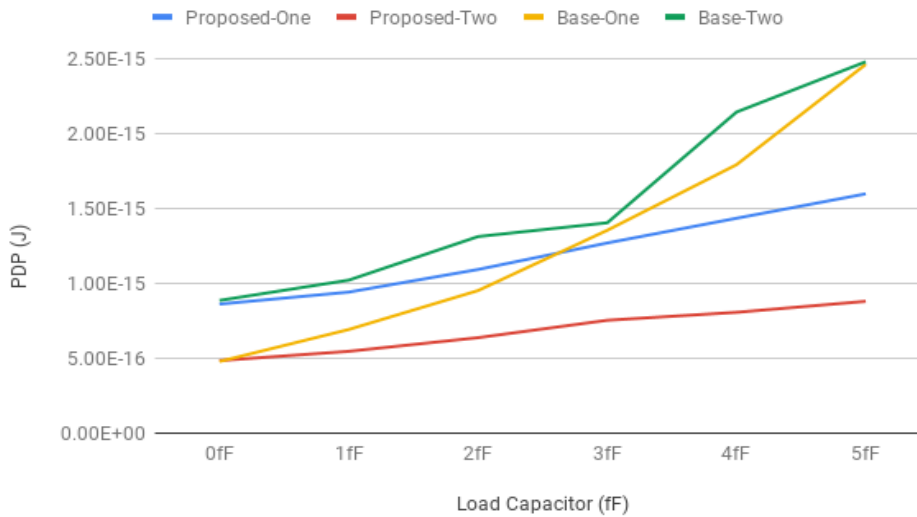Figure 10. Diagram of power consumption versus load capacitance (at the output)

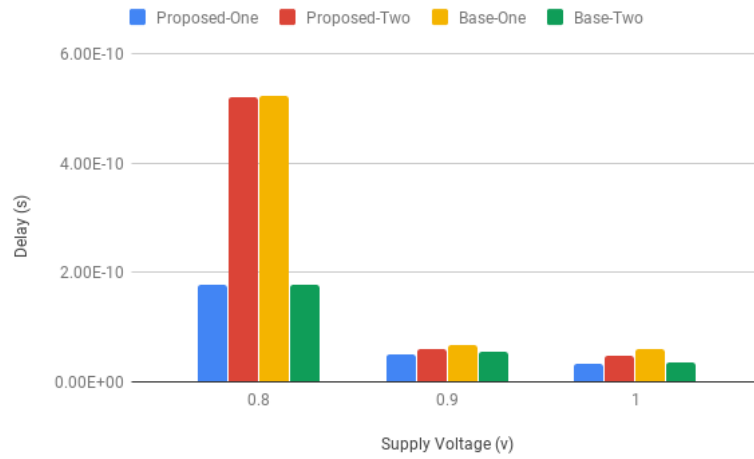Figure 11. Diagram of PDP versus load capacitance (at the output)
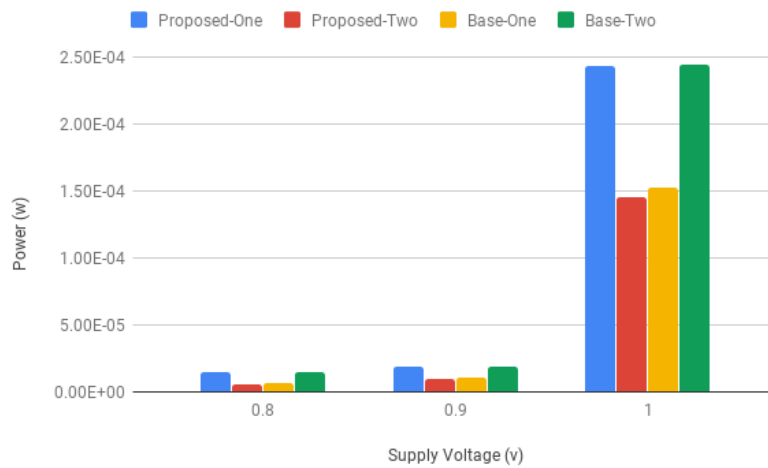
Figure 12. Diagram of delay versus Supply voltage

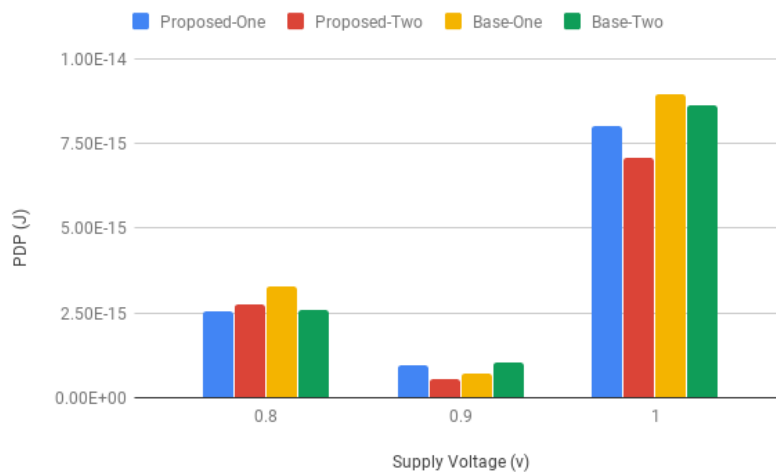

Figure 13. Diagram of Power versus Supply voltage

Figure 14. Diagram of PDP versus Supply voltage

7. Conclusion
This paper proposed two CNFET-based ternary full adder circuits with lower design complexity and better power consumption, delay and PDP than the state-of-the-art ternary full adders based on CNFET technology. The proposed designs generate all of the required logical levels with a single power supply. The designs were simulated in the software HSPICE 2014 using the Stanford University

CNFET library based on 32-nm technology. In these simulations, load capacitances of 0 to 5fF were placed at the circuit output, and the effects on performance were investigated. The diagrams obtained from the simulations demonstrate the stability of the proposed designs.

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